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COOK, ALEX, MCFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
Suite 2850
200 West Adams St.
Chicago, IL 60606

EXAMINER	
PHAM, THANH V	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Application Number: 09/768,133
Filing Date: January 23, 2001
Appellant(s): NAGAO ET AL.

Mark J. Murphy
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/19/2007 appealing from the Office action mailed 03/20/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The Appeal Brief of related application serial No. 10/951,065 filed on the same day of 9/19/2007 as of this Appeal Brief. The 10/951,065 application claims the devices while this application, 09/768,133, claims the methods of fabricating those devices.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Appellant's admitted prior art in combination with

5,453,406	Chen	9-1995
5,550,066	Tang et al.	8-1996
5,990,988	Hanihara et al.	11-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 31, 33, 35-41, 43-50, 52-59, 61-68, 70-77, 79-86, 88-91, 93-95, 97-101, 103-105, 107-111, 113-115, 117-121, 123-125, 127, 129-131, 133-135, 137, 139-141, 143-145, 147, 149-152, 154-156, 158, 161-164, 166-168, 170, 173-176, 178-180, 182, 185-196 and 197-205 are rejected under 35 U.S.C. 103(a) as being unpatentable over Appellant's admitted prior art in combination with Chen U.S. Patent No. 5,453,406, Tang et al. US 5,550,066 and Hanihara et al. US 5,990,988.

The Appellant's admitted prior art for the TFT formation to form a display device having pixel electrodes and an insulative layer over the pixel electrodes is similar to the instant invention, having use of an organic material where a low dielectric property is considered (the instant specification, pages 1-2 and 7).

> An active matrix liquid crystal display device is widely used for OA equipment, television sets and the like.
>
> The substrate is spun so that the varnish is uniformly applied thereto. The substrate on which the varnish is applied is baked in an oven or on a hot plate to obtain an insulating film.

The thickness of the insulating film is controlled by the number of spinnings, the period of spinning time, the concentration and the viscosity of the varnish. A material used for spin-coating can be selected from a polyimide resin, an acrylic resin, a resin containing a siloxane structure, an inorganic SOG (Spin on Glass) material and the like, in consideration of physical properties such as a transparence, a heat resistance, a chemical resistance, and a thermal expansion coefficient. In the case where a low dielectric property is considered as an important factor, an organic material is often used.

FIG. 2 shows a cross section of a conventional active matrix substrate. On a glass substrate 100, level differences generated by an active layer (including a channel region 101, a source region 102, and a drain region 103), a gate wiring 105, a source wiring 107, a drain wiring 108 and the like are present. A leveling resin, representatively an acrylic resin, is used to as a first leveling film 109 so as to level these level differences. Finally, a pixel electrode 111 is formed on the first leveling film 109 to complete the active matrix substrate.

Next, as shown in FIG. 3, the active matrix substrate is bonded to a counter substrate 120 so as to interpose liquid crystal 123 therebetween to form a liquid crystal display device. According to this conventional method of forming a leveling film, however, it is apprehended that the pixel electrode 111 might be broken because of insufficient flatness of the leveling film. Moreover, since the unevenness due to the level differences remains on the surface of the pixel electrode 111, poor orientation of the liquid crystal 123 is caused on the uneven region of the surface.

As being seen in fig. 2, the wiring is connected to the semiconductor film through a first hole in the interlayer insulating film on the interlayer insulating film and the pixel electrode is connected to the wiring through a second hole. In Appellant's admitted prior art fig.3, an electro luminescence layer 112 is formed over the pixel electrode 111.

In the Summary of the Invention, the instant specification states, "a TFT is formed in a similar manner as in the prior art shown in Fig. 2".

<u>The Appellant's admitted prior art lacks</u> the second leveling layer over the first leveling layer.

The Chen reference discloses a method for producing a planar surface (col. 2, lines 64-67) wherein the thickness of a first leveling film 40 (2,000-3,000 Angstroms, col. 6, lines 1-10) formed above a wiring 34 is thinner than that of a second leveling film 42 (4,000-6,000 Angstroms, col. 6, line 53-54) formed on the first leveling film. Both first and second leveling films are formed by spin coating and by the same material (col. 6, line 30). The method could be used to coat a display device.

In Chen's fig. 7, a second spin-on-glass layer 42 is formed over the first spin-on-glass layer 40 essentially planarizing the dielectric layer and completing the process. This second spin-on-glass layer 42 is formed by also using the liquid precursor of the siloxane type similar in composition to the material used for the first spin-on-glass layer 40, but in this second coating the spin-on-glass is dispensed at a significantly higher spin speed and at a constant speed. The same series of spin-on-glass is used for both layers.

There are three consecutive sections related to the insulating layer and the first and second spin-on-glass layers.

The first section in col. 5, lines 50-60 teaches the formation of the insulating layer 36 with "<u>the preferred thickness of the insulating layer 36 is between about 2000 to 4000 Angstroms</u>".

The second section, from col. 5, line 61 to col. 6, line 24, teaches the formation of the first spin-on-glass layer 40 with "more specifically the **preferred** spin-on-glass material is a series of siloxane base material" with an example of using series 211 which "<u>produce a thinner coating of about 2000 Angstroms</u> while series 314 and 311

have a higher viscosity and produce coatings of about 3000 Angstroms" in the conditions of

> First bringing the substrate to a constant rotational speed in the range of about 600 to 800 revolutions per minute (rpm) and then dispensing the spin-on-glass liquid precursor for about 6 seconds. The spin-on-glass is then allowed to air dry at room temperature of about 25 ^{O}C **for another 15 second at the above constant rotational speed**. The substrate is then removed from the spin coater and baked, for example on a hot plat, at a temperature of between about 100 to 300 for a time of between 0.5 to 2.0 minutes, because of this lower and constant spin speed the recesses or gaps between the patterned conductor 34 fill more evenly, as was depicted earlier in FIGS. 3A and 3B.

The third section in col. 6, lines 25-55 teaches the formation of the second spin-on-glass 42 in the conditions of "this second spin-on-glass layer 42 is formed by also using the liquid precursor of the siloxane type similar in composition to the material used for the first spin-on-glass layer 40, but in this second coating the spin-on-glass is dispensed at a significantly higher spin speed and at a constant speed" wherein

> The substrate is again placed on a spin coater and brought to a constant rotational speed in the range of about 2500 to 3000 revolutions per minute (rpm) before dispensing the spin-on-glass and then the substrate is maintained at this constant rotational speed for an additional 6 seconds. **The substrate is then brought to a stationary position, that is the spin speed is reduced to zero rpm** and the second spin-on-glass is allowed to air dry at room temperature of about 25 ^{O}C for an additional 15 seconds. The substrate is them baked, for example on a hot plate, at a temperature of between about 100 to 300 ^{O}C for a time of between about 0.5 to 2.0 minutes, the spin-on-glass layer 42 is then pyrolyzed at a relatively high temperature to form an inorganic glass. The preferred curing temperature for this last step is between about 400 to 500 ^{O}C and for a time of about 20 to 30 minutes, and more specifically at a temperature of 425 ^{O}C for 30 minutes thereby forming the inorganic glass. The **preferred** thickness of layer 42 is between about 4000 to 6000 Angstroms as can be seen in FIG. 7, the spin-on-glass dielectric layer fills the recesses and essentially planarizes the irregular recesses or gaps on the substrate.

It is clear that with the same composition put in different conditions, the thickness of the two spin-on-glass layers have different thickness. The example in the above second section in the formation of the first spin-on-glass/leveling layer 40 is about 2000 or 3000 Angstroms. The given thickness of the preferred series 211, 314 or 311 <u>while teaching the first spin-on-glass formation</u> is obviously the preferred thickness for that layer. The preferred thickness of layer 42 is not 2000 or 3000 Angstroms but preferred to be up to 4000 to 6000 Angstroms, thicker than the previous spin-on-glass layer.

Further, in Chen's fig. 7, the first 'leveling' layer 40 is thicker than the second 'leveling' layer 42 at some positions; and also in other positions, the second leveling layer 42 is thicker than the first leveling layer 40 at other positions in the same manner as it as in instant's fig. 1 or fig. 4.

*Thus, one of ordinary skill in the art could chose from the provided ranges to have the second leveling film thicker than the first leveling film as a matter of routine experimentation based on those provided ranges. Choice of thickness of the leveling layers would <u>further depend on many other factors</u> such as the <u>gap</u> between the protruded elements or the <u>height of the protruded element</u> and would be obtained by routine experimentation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the appropriate thickness such as the thickness in the ranges as claimed having the second leveling film thicker than the first leveling film into the process as the **<u>overall</u>** thicknesses would be selected in accordance with the surface planarity formation as taught by Chen.*

<u>The Chen reference further discloses</u>, col. 5, lines 24-29

> insulating layer 36 is deposited thereon (on devices' conducting layers) by conventional means. For example, the insulating layer can be composed of silicon dioxide and silicon nitride and deposited using CVD or LPCVD.

and col. 6, line 67 to col. 7, line 15

> Although this embodiment describes a process for forming a single planar dielectric layer over a single patterned conducting layer, it should also be well understood by one skilled in the art that the process can be repeated to form additional patterned metal layers having planarized dielectric layer formed thereon. This can be accomplished by first depositing a second insulating barrier layer over the cured second spin-on-glass layer 42, forming via hole openings in the planar dielectric layer to the underlying conducting layer and then depositing a second conducting layer, such as aluminum, which contacts the first conducting layer through the via holes, the conducting layer can then be patterned by reactive ion etching and then planarizing process ARIC SOG of this invention can be used to planarize the second level metal. By repeating this process by the above method a multilayered metallurgy can be fabricated.

The passivating layer of an insulating material such as silicon oxide (Tang et al., col. 7, line 30), silicon nitride or silicon oxide (Chen, col. 5, lines 24-27) as same as "Specific insulators include noncrystalline compounds such as silicon oxide, silicon nitride, or silicon nitride oxide," Nishimura et al. US 6,332,835, col. 7, lines 64-6 and/or "the insulating film formed on the data line, not only an oxide film, but also a nitride film or oxide-nitride film may be used", Tsuji et al. US 5,821,622, col. 27, lines 2-4, is well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the Appellant's admitted prior art with the second leveling layer as taught by Chen because the second leveling layer of Chen would provide the prior art structure with planarity over the formed TFT to prevent the pixel electrode from rough topography and improve the optical resolution (Chen's col. 1, lines

18 and 29). With this combination, the pixel electrode would be connected to the wiring through a second hole formed in the passivating/insulating film (of silicon nitride, silicon oxide nitride or silicon oxide as well-known in the art) and the leveling film on the wiring as claimed.

Re claim 8, the Appellant's admitted prior art discloses the driving TFT section but not the section of pixel TFT for controlling electric current to the EL element therefore it does not show the EL cathode. However, the formation of a cathode made of a conductive film having a light shielding property is known in the art as EL cathode 84 in the Tang et al.'s figs. 3 and 9 and the associated passages. The Tang et al. reference also teaches "a passivating layer 74 of an insulating material, preferably silicon dioxide, is deposited over the surface of the device (the wiring 62/72)", col. 7, lines 30-35.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the formation of a cathode made of a conductive film having a light shielding property of Tang et al. because the formation of a cathode made of a conductive film having a light shielding property of Tang et al. would provide the method of the combination with sufficiently low temperature fabrication (abstract and col. 2, line 61, e.g.)

The Appellant's admitted prior art does not disclose the wiring is a three-layered laminated film containing a first titanium, an aluminum film and a second titanium film. The Hanihara et al. reference teaches "the wiring layers 31, 32, 33 and the pixel electrode layer 34 are films made of such conductive metals as ... layers of titanium and

aluminum formed by sputtering or evaporation or photolithography" (col. 6, lines 18-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the layers of titanium and aluminum as taught by Hanihara et al. because the layers of titanium and aluminum for the wiring would provide the device formed by the combination with controllability (col. 1, line 9).

(10) Response to Argument

The rejection is based on Appellant's admitted prior art in combination with Chen *and optimization* for the main idea. One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation to achieve desired device dimensions and associated device properties and desired device density on the finished wafer. Appellant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

The main issue in the argument is about the Chen reference's two spin-on-glass layers 40 and 42, which are alleged that the first is not thinner than the second. The response is as follow:

First, if all other conditions/parameters/variables besides spinning speeds are kept the same, the examiner would accept Appellant's argument(s). However, in this case, *a crucial parameter is absent or not disclosed, thereby, all parameters are not the same.*

Second, the two spinning speeds of the two layers are agreed as in the range of the provided information, the Honeywell literature, on page 25 of Appellant's argument. However, there is a change of variable during time as taught by Meyerhofer (provided by Appellant's in the last IDS, filed 08/18/2006, mentioned in the argument's page 24) "[T]he thickness, of course, decreases continuously with time as material is spun away", col. 1 page 3993.

Third, the two spinning speeds for the first layer 40 and the second layer 42 of Chen in 5,453,406 are "not very high (<6000 rpm)", as taught by Lai, first col. of page 1119 (also provided by applicant in the last IDS, *and not mentioned to in this Appeal Brief's Argument anymore*). Further, Lai teaches, "the spinning time to 15 s., which is the approximate time required to slough off the bulk of the polymer solution", same col. of page 1119. Applying this teaching, the first layer 40 is dried out at the constant 600-800 rpm which is the spin-on-glass material being continuously spread for another 9 sec. (after the first 6 sec. of dispensing) and then slough off the applied surface for at least the remaining 6 sec. as taught by Chen; meanwhile the second layer 42 is dried

out at zero rpm being neither spread nor slough off. The first coating 40 is spun at a higher speed than the second coating 42 during the drying step.

Four, it is not by change or by accident that the thickness of the forming layer of 2000 or 3000 angstroms being mentioned during the description of the step of forming the first spin-on-glass coating 40 in Chen; i.e., the *intended* thickness of the formed first spin-on-glass coating 40 would be 2000-3000 angstroms (Chen 's col. 6, lines 7-10) in compared with the "*preferred* thickness of layer 42 is between about 4000 to 6000 Angstroms" (Chen 's col. 6, lines 53-54). Though, the first spin-on-glass coating in Chen is the same as the Honeywell literature for a common applied material.

Five, Chen also discloses "because of this lower and constant spin speed the recesses or gaps between the patterned conductor 34 fill more evenly, as was depicted earlier in FIGS. 3A and 3B" (col. 6, lines 22-23) which would compensate for the thickness of the formed film in the recess/gap and on the protruding elements.

Therefore, the first spin-on-glass coating 40 would be thinner than the second spin-on-glass coating 42 of Chen used in the rejection (*in combination with the routine experimentation for optimization*) and as same as the claimed invention.

Further, in Chen's fig. 7, the first 'leveling' layer 40 in the trenches is thicker than the second 'leveling' layer 42 directly upon it in some locations; and *in other locations, the first 'leveling' layer 40 in the trenches is thinner than the second 'leveling' layer 42 directly upon it* as it as in instant's fig. 1 or fig. 4. The following figures, copied from instant drawings and Chen's, with marks showing the differences in thickness would provide clearer explanation.

Zone where the first leveling film is thicker than the second leveling film

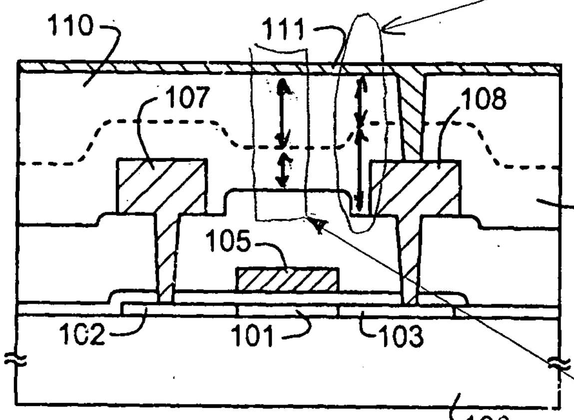

FIG. 1

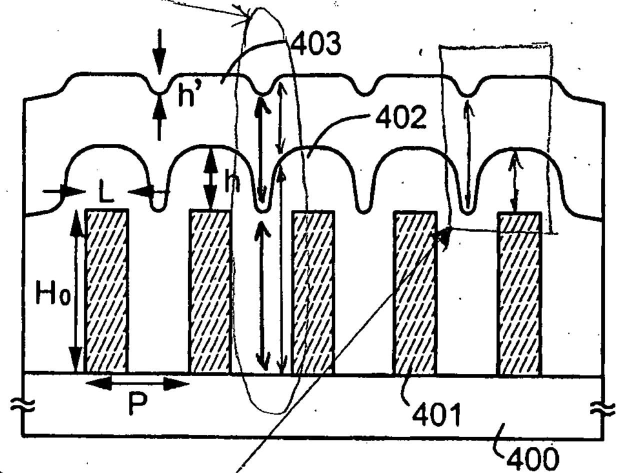

FIG. 4

Zone where the second leveling film is thicker than the first leveling film

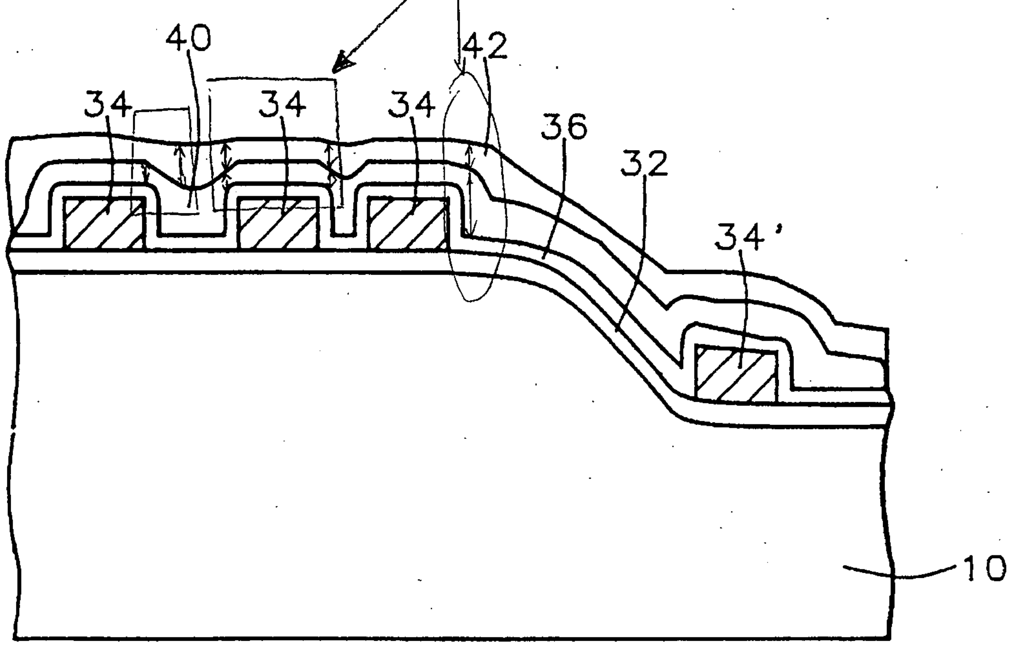

FIG. 7

The figures do not specify where T_1 or T_2 (thickness of the first leveling film or the second leveling film, respectively) is located. In this instant, the figures should be objected to under 37 CFR 1.83(a): the drawings must show every feature of the invention specified in the claims; the thicknesses must be shown or the feature(s) canceled from the claim(s). The examiner regrets that the objection to the figures is not made in previous office action(s).

It is appreciated that appellant spends time to analyze the different thicknesses of applied layers; however, appellant does not provide any indicating where each thickness is, i.e., where T_1 or T_2 stands amongst many elements in instant figs. 1 or 4. With that lacks of information, in the above rejection, the examiner states "*[C]hoice of thickness of the leveling layers would <u>further depend on many other factors</u> such as the <u>gap</u> between the protruded elements or the <u>height of the protruded element</u> and would be obtained by routine experimentation*", "*one of ordinary skill in the art at the time the invention was made to apply the appropriate thickness such as the thickness in the ranges as claimed having the second leveling film thicker than the first leveling film into the process as the overall thicknesses would be selected in accordance with the surface planarity formation as taught by Chen*".

In response to appellant 's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was

within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this instance, the combination based on the appellant's admitted prior art teaches substantially all of instant invention, lacks the second leveling layer thus the pixel electrode, a metallurgy layer formed afterward, does not planar; and the Chen reference teaches forming two leveling layers for the sake of planar surfacing such that improves multilayer metallurgy to wire up the discrete devices on the integrated circuit chip (Chen's col. 1, lines 18 and 29) which is happened the same purpose as of claimed invention's purpose in such a manner that it does not teach away the invention. The combination is clearly not based on improper hindsight and therefore the reconstruction is proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thanh Van Pham

Conferees:

Matthew Smith

Darren Schuberg